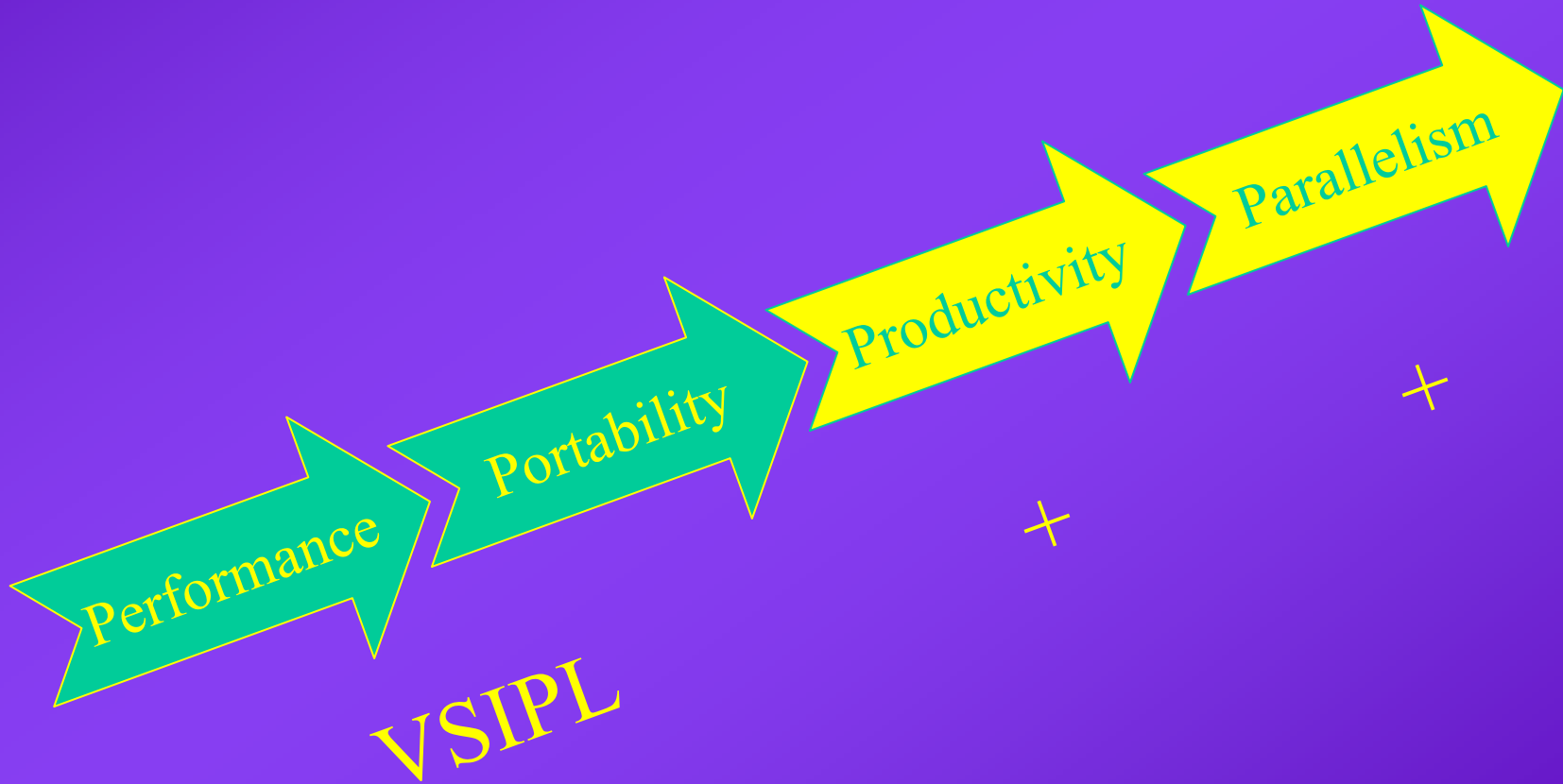




# Serial and Parallel Performance

CodeSourcery, LLC  
September 23, 2003

# Design Path



# Specification Status

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- **Serial Specification**
  - 216-page draft.
  - Under review by VSIPL Forum.
- **Parallel Specification**
  - 24-page preliminary draft.
  - Initial conceptual review complete.

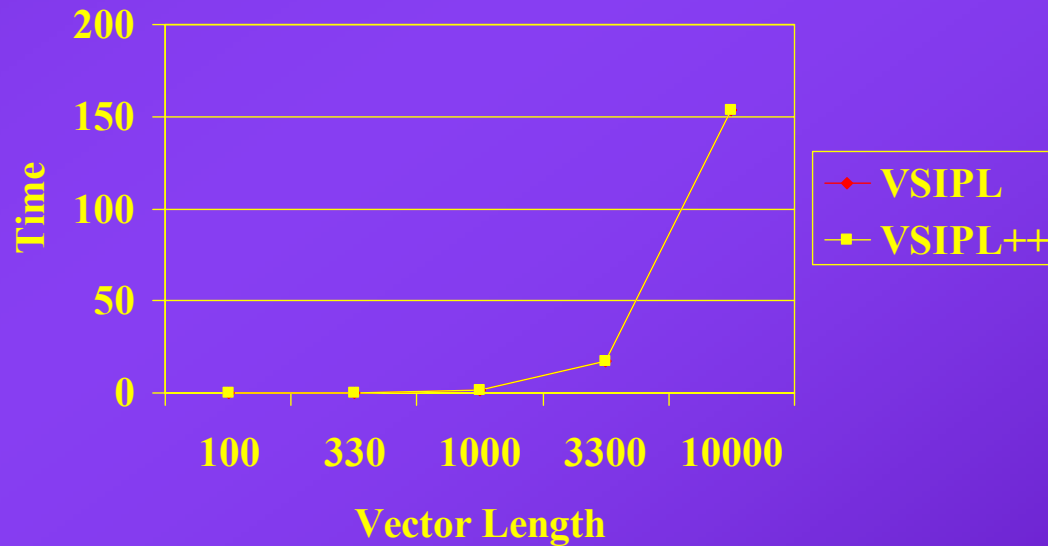
# Serial Performance

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- Uses VSIPPL reference implementation.
  - Not the fastest implementation...
  - ... but the relative performance is important.
- Environment:
  - 2GHz Pentium-M
  - 512KB cache, 512MB RAM
  - GNU/Linux, G++ 3.4

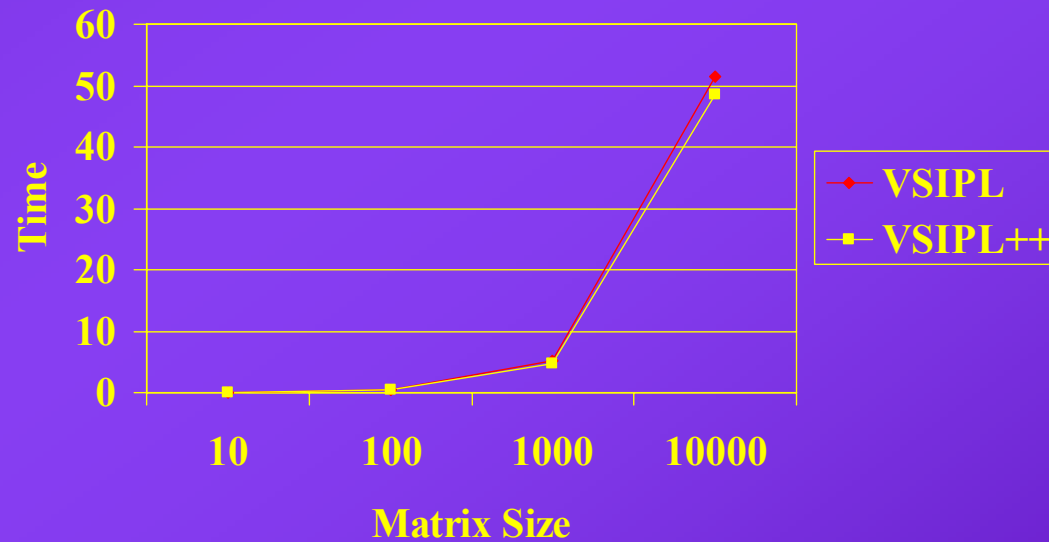
# Matrix/Vector

$v += mv$

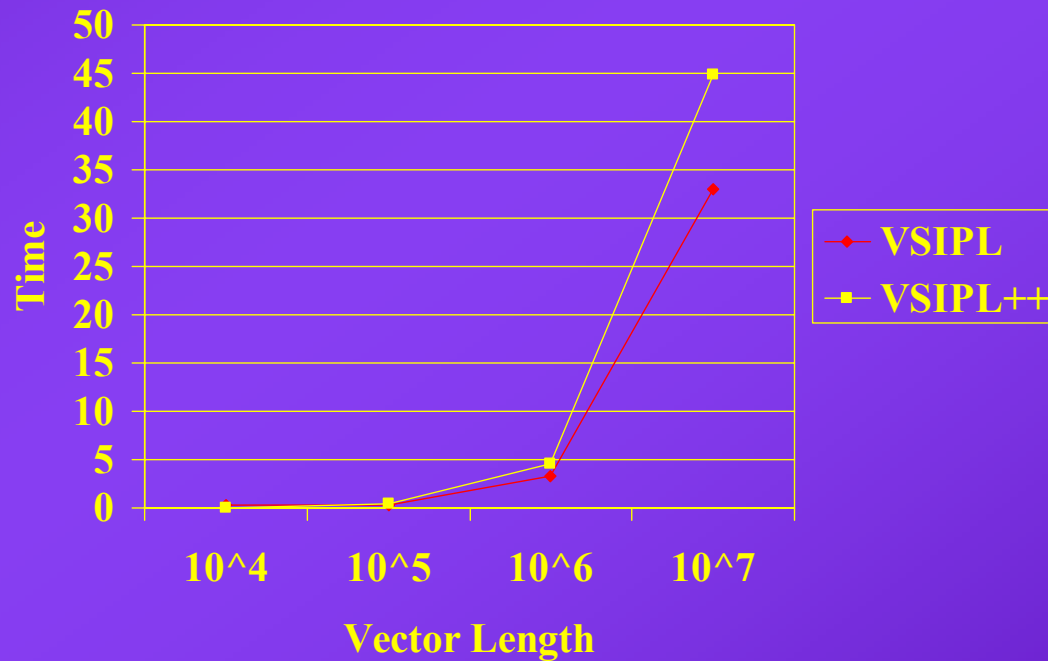


# Matrix/Matrix

`result += tan(sin(m) + cos(m))`



# Checked Vector Access



# Performance Conclusions

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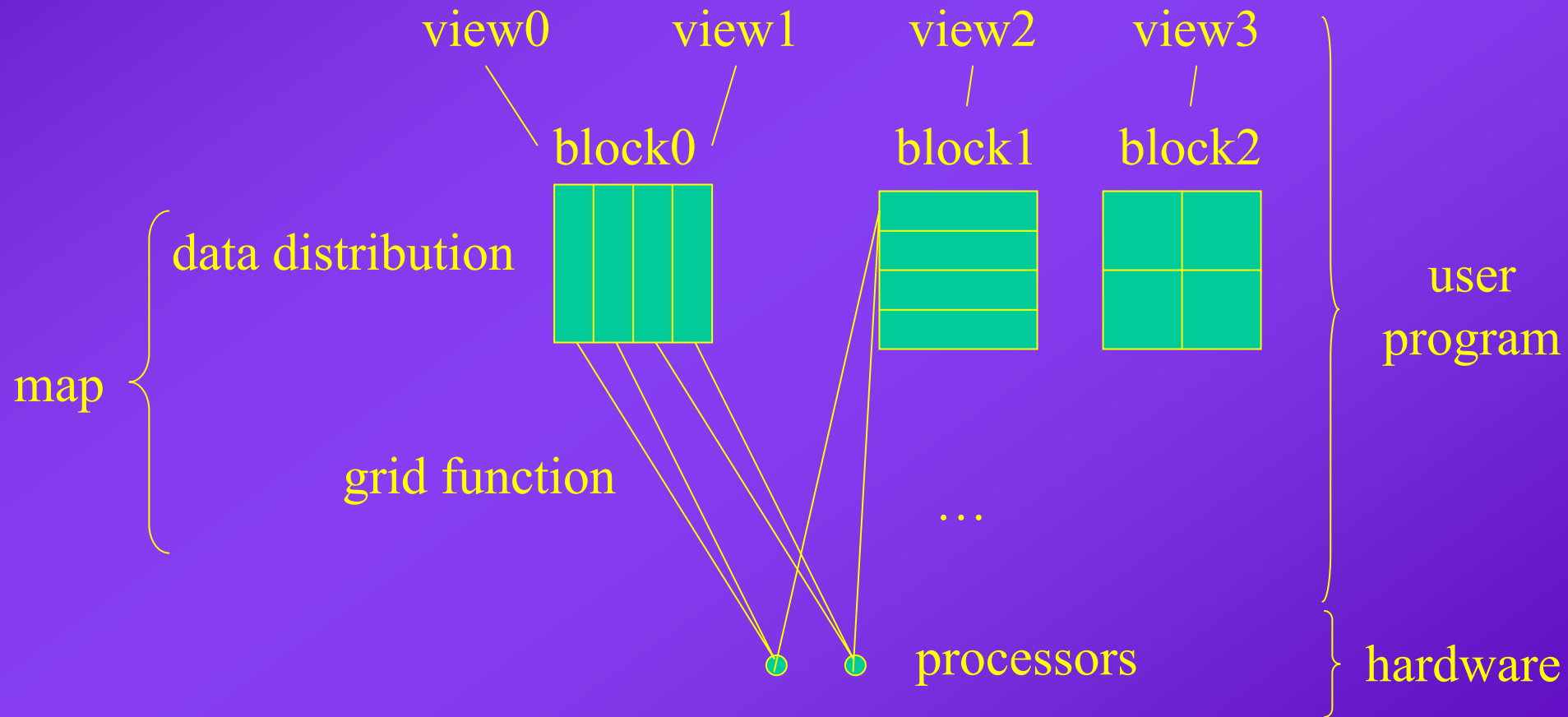
- VSIPL++ has approximately zero overhead.
  - Memory effects actually enable VSIPL++ to outperform VSIPL.
  - Expression-template techniques may also improve performance.
- Exceptions are expensive.
  - We are not sure if this overhead can be eliminated.
- Reference implementation will be directly useful.
  - Vendor-optimized versions will probably be better.

# Parallelism

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- Target systems:
  - Support 1-64K+ processors.
  - Support MPI, POSIX threads.
- Conceptual model:
  - Single-program multiple-data model.
  - Owner computes.
  - Parallelism requires changing only declarations, not expressions.

# Parallel VSIPL++ Model



# Using Parallelism

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- Declaration:

```
Vector<double,  
        Dense<1, double,  
             Map<Block> > >  
v (17, 1.0, Block(4));
```

- Meaning:

- 17: Vector length.
- 1.0: Initial value.
- Block(4): Block distribution over 4 processors.

# FYO4 Objectives

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- **Specification:**
  - Finalize serial and parallel specifications.
  - Get approval from VSIPL Forum.
- **Implementation:**
  - Finish serial implementation.
  - Draft parallel implementation.
- **Measurement:**
  - Performance analysis.

# Contact Information

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